Claims

1. A method for efficiently processing layers of a data packet, comprising:

defining a pipeline of processors in communication with a distributed network and a central processing unit (CPU) of a host system;

receiving a data packet from the distributed network into a first stage of the pipeline of processors;

processing the data packet to remove a header associated with the first stage;

transmitting the processed data packet to a second stage for processing associated with the second stage;

repeating the operations of processing the data packet and transmitting the processed data packet for successive stages until a header associated with a final stage has been removed from the data packet; and

transmitting the data packet from the final stage to the CPU of the host system.

2. The method of claim 1, wherein the data packet is an Ethernet data packet.

3. The method of claim 1, wherein each processor of the pipeline of the pipeline of processors includes at least three buffers configured to maintain a line rate.

4. The method of claim 1, wherein the successive stages correspond to layers of the data packet.

5. The method of claim 4, wherein the layers are selected from the group consisting of an IP layer, an IP SEC layer, a TCP layer, and an ISCSI layer.

6. The method of claim 1, wherein the method operation of processing the data packet to remove a header associated with the first stage includes,

defining instructions for processing the data packet; and

enabling an arithmetic logic unit (ALU) associated with each processor to process the instructions.

7. The method of claim 6, wherein the method operation of enabling an arithmetic logic unit (ALU) associated with each processor to process the instructions includes,

aligning the instructions by a least significant bit; and

extending each of the instructions to a defined bit size.

8. An adapter card configured to be in communication with a general purpose computer, comprising:

a plurality of processors arranged in a pipeline architecture, the plurality of processors defining a receiving pipeline and a transmitting pipeline, each of the plurality of processors associated with a pipeline stage, each pipeline stage configured to process a

layer of a data packet, wherein the receiving pipeline removes layers from the data packet and the transmitting pipeline adds layers to the data packet.

9. The adapter card of claim 8, wherein the pipeline stage is associated with a layer of an Ethernet packet header.

10. The adapter card of claim 9, wherein the layer is selected from the group consisting of an IP layer, an IP SEC layer, a TCP layer, and an ISCSI layer.

11. The adapter card of claim 8, wherein the adapter card is a network interface card.

12. The adapter card of claim 8, wherein each of the plurality of processors include at least three buffers for maintaining an incoming line rate.

13. The adapter card of claim 8, wherein each of the plurality of processors include alignment circuitry configured to align a lowest significant bit of an operand, the alignment circuitry extending the operand to a defined bit width so that a pre-extending bit width of the operand is transparent to an arithmetic logic unit configured to process the operand.

14. A general purpose computer, comprising:

a central processing unit (CPU);

a network interface card (NIC) configured to process data packets, the NIC including,

a plurality of processors arranged in a pipeline architecture, the plurality of processors defining a receiving pipeline and a transmitting pipeline, each of the plurality of processors associated with a pipeline stage, each pipeline stage configured to process a header associated the data packets, wherein the receiving pipeline removes headers from the data packets and the transmitting pipeline adds headers to the data packets.

15. The general purpose computer of claim 14, wherein the pipeline stage is associated with a layer of a header of the data packets.

16. The general purpose computer of claim 15, wherein the layer of the header of the data packets is selected from the group consisting of an IP layer, an IP SEC layer, a TCP layer, and an ISCSI layer.

17. The general purpose computer of claim 14, wherein each of the plurality of processors have at least three buffers configured to maintain an incoming line rate.

18. The general purpose computer of claim 14, wherein each of the plurality of processors include alignment circuitry configured to align a lowest significant bit of an operand, the alignment circuitry extending the operand to a defined bit width so that a

pre-extending bit width of the operand is transparent to an arithmetic logic unit configured to process the operand.

19. The general purpose computer of claim 14, wherein each of the plurality of processors are configured to execute a two stage pipeline process.

20. The general purpose computer of claim 14, wherein each of the data packets have a variable packet size.